

ENGR 2218 – DIGITAL LOGIC

Fall 2019

Syllabus

Instructor: Bill Saari

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Office Hours: 11:00am - 12:50pm on Mondays; 11:00am - 11:50am on Tuesdays, Wednesdays, and Thursdays

Course Website: <http://www.ar.cc.mn.us/saari/engr2218>

Course Description

Topics include logic gates, number systems, Boolean Algebra, combinational logic, Karnaugh Maps, flip-flops, counters, registers, and programmable logic using VHDL. Laboratory included.

Prerequisite

Math 1400

Major Areas of Course Content

1. Logic gates
2. Number systems
3. Boolean Algebra
4. Combinational logic
5. Karnaugh Maps
6. Flip-flops
7. Counter
8. Registers
9. Programmable logic using VHDL

Learner Outcomes

1. Comprehend and apply fundamental engineering concepts related to digital logic
2. Present clear and accurate solutions with respect to mathematics
3. Construct, test, and analyze digital circuits in a laboratory setting

Textbook

Fundamentals of Logic Design by Roth and Kinney, 7th Edition

Grading

Grades will be determined based on a weighted average of percentages.

Exams: 4 of 5 exams (the lowest exam score will be dropped) x 20% = 80%

Labs: 20%

A > 90%, B > 80%, C > 70%, D > 60%, F < 60%

Exams

Exams will be closed book, closed notes, and you will not be allowed to use calculators. Exam 5 will be during the final exam week, and will be cumulative and multiple choice. There will be no make-up exams under any circumstance. To account for an emergency on an exam date, your lowest exam score will be dropped.

Homework

Homework will be assigned on a regular basis. Homework will not count towards your grade, but it is critical that you do all of the homework problems. You can submit your homework to me if you would like feedback on your work.

Academic Dishonesty

You are encouraged to work with others in the class. However, I expect the work you submit to be your own efforts. Instances of academic dishonesty will be dealt with according to the regulations of Anoka-Ramsey Community College.

Class Conduct

You are expected to be courteous towards the instructor and your classmates. You are expected to be on time for lecture and lab. Cell phones should be put away during lecture. You should not talk to your classmates while I am talking or while one of your classmates is asking a question. If you have a question about the course material, ask me and I will be more than happy to answer your question. The instructor reserves the right to take any necessary action for class disruptions in accordance with the Student Handbook.

Tentative Course Schedule

Week of	Topics	Book Chapters
Aug 26	Number Systems and Conversion	Unit 1
Sep 2	Number Systems and Conversion No Class: Monday, September 2	Unit 1
Sep 9	Number Systems and Conversion	Unit 1
Sep 16	Basic Logic Gates Exam 1: Friday, September 20	Unit 2
Sep 23	Boolean Algebra Minterm and Maxterm Expressions	Unit 2 Unit 4
Sep 30	Karnaugh Maps	Unit 5
Oct 7	Additional Logic Gates and Applications Exam 2: Wednesday, October 11	Units 3 and 7
Oct 14	Combinational Logic No Class: Friday, October 18	Unit 8
Oct 21	VHDL	Unit 10
Oct 28	Multiplexers and Decoders	Unit 9
Nov 4	Latches and Flip-Flops Exam 3: Friday, November 8	Unit 11
Nov 11	Latches and Flip-Flops No Class: Monday, November 11	Unit 11
Nov 18	Latches and Flips-Flops Registers and Counters	Unit 11 Unit 12
Nov 25	Registers and Counters No Class: Friday, November 29	Unit 12
Dec 2	Registers and Counters Exam 4: Thursday, December 5	Unit 12
Dec 9	Review	
Exam 5: Wednesday, December 18, 9:40 – 11:40 am		