ENGR 2218 – DIGITAL LOGIC
Fall 2008
Syllabus

Instructor: Bill Saari
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Office Hours: MWF 12-12:50, T/H 11-11:50
Course Website: http://www.ar.cc.mn.us/saari/engr2218

Course Description: Introduction to the fundamentals of digital circuit analysis and design. Covers logic gates, Boolean algebra, Karnaugh Maps, mathematical operations, flip-flops and counters. Laboratory included.

Pre-requisites: Math 1400, Phys 1127 or concurrent enrollment
Textbook: Digital Fundamentals with VHDL by T. L. Floyd

Grading:
4 Exams: 4 x 20% = 80%
Labs: 20%

A > 90%, B > 80%, C > 70%, D > 60%, F < 60%

Exams: Exams will be closed book, closed notes, and you will not be allowed to use calculators. There will be no make-up exams except under extreme cases determined at the discretion of the instructor, and only one make-up exam will be allowed. In order to be even considered for a make-up exam, you must contact me on or prior to the scheduled date for the exam.

Homework: Homework will be assigned on a regular basis. Homework will not count towards your grade, but it is critical that you do all of the homework problems. You can submit your homework to me if you would like feedback on your work.

Academic Dishonesty: You are encouraged to work with others in the class. However, I expect the work you submit to be your own efforts. Instances of academic dishonesty will be dealt with according to the regulations of Anoka-Ramsey Community College.

Class Conduct: You are expected to be courteous towards the instructor and your classmates. Class disruptions include: arriving late for lecture and lab, talking during lecture with other students, and cell phones not turned off during lecture. These and other class disruptions will be dealt with in accordance with the Student Handbook.

Tentative Course Schedule

Week of	Monday	Wednesday	Friday
Aug 25	Ch. 1	Ch 1	Ch 2
Sep 1	**No Class**	Ch 2	Ch 2
Sep 8	Ch 2	Ch 3	Ch 3
Sep 15	Ch 3	Ch 4	Ch 4
Sep 22	**Exam 1**	Ch 4	Ch 4
Sep 29	Ch 4	Ch 4	Ch 4
Oct 6	Ch 5	Ch 5	Ch 6
Oct 13	**Exam 2**	Ch 6	**No Class**
Oct 20	Ch 6	Ch 6	Ch 6
Oct 27	Ch 6	Ch 6	Ch 8
Nov 3	Ch 8	Ch 8	Ch 8
Nov 10	Ch 8	Ch. 8	Ch 9
Nov 17	**Exam 3**	Ch 9	Ch 9
Nov 24	Ch 10	Ch 10	**No Class**
Dec 1	Ch 13	VHDL	VHDL
Dec 8	VHDL	VHDL	VHDL
Exam 4: Tuesday, December 16, 8:30-9:30am			