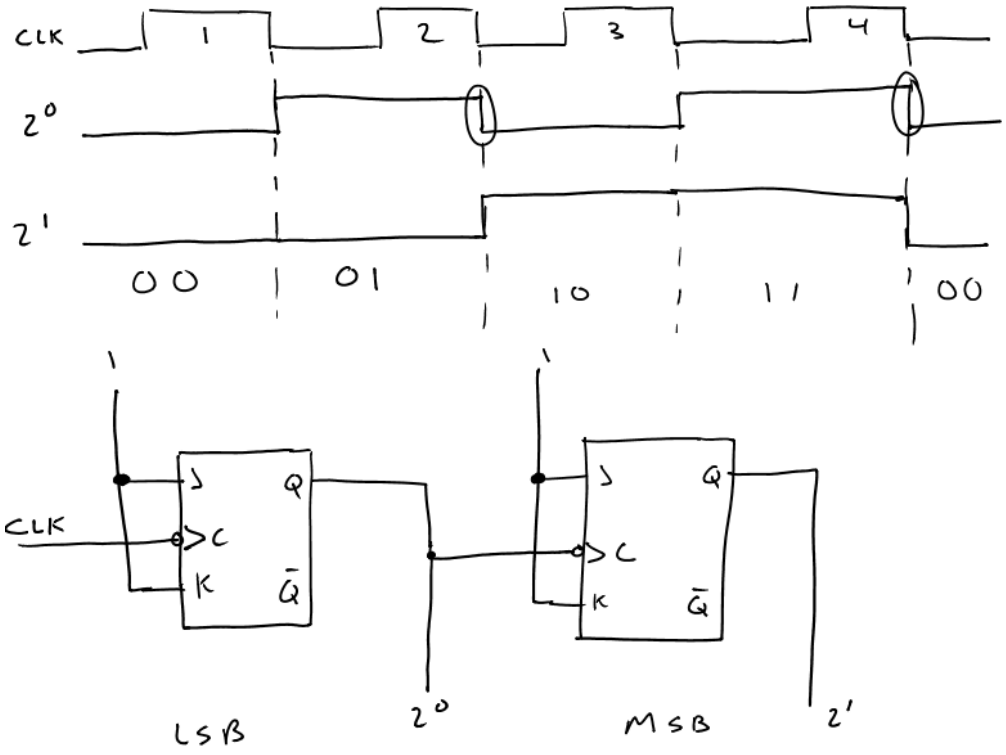
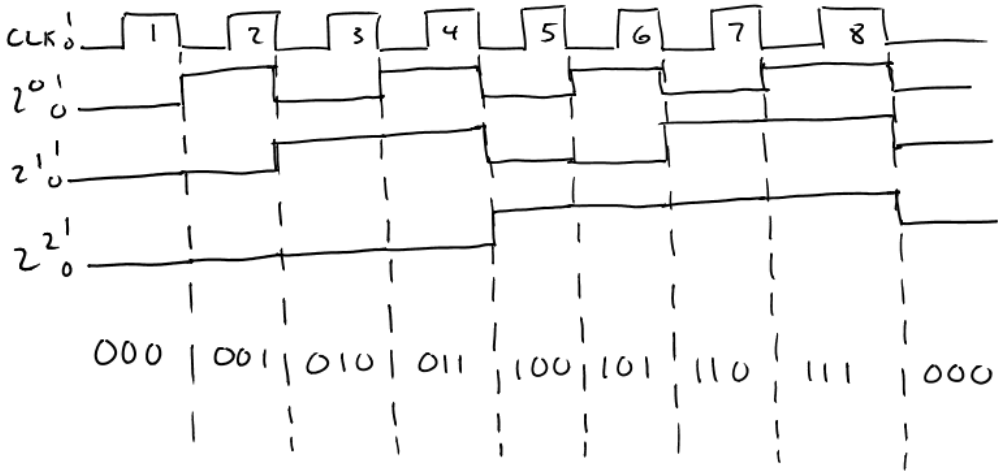
Counters
- Counts the pulses in a clock waveform
- Uses J-K Flip-Flops

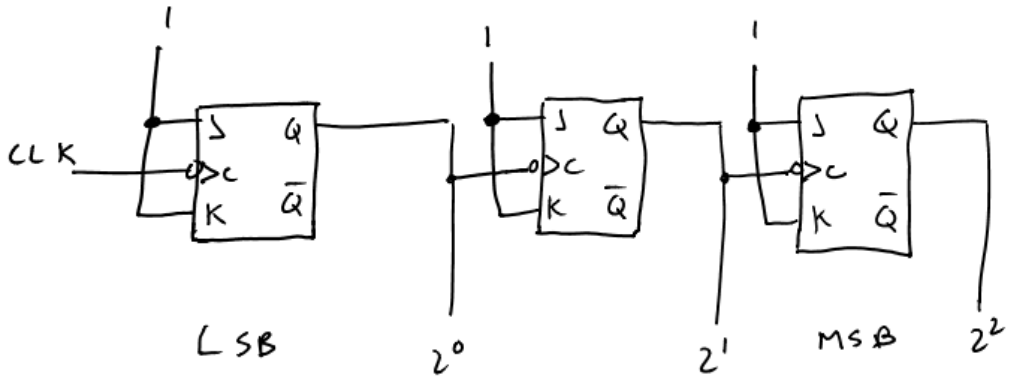
Asynchronous (Ripple) Counters
- Not all Flip-Flops trigger based on the clock

2-bit

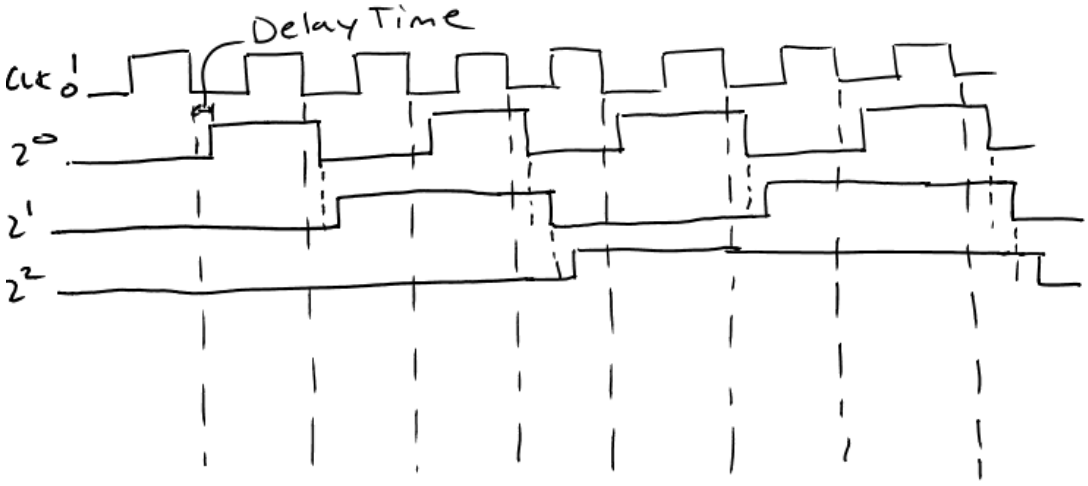


3-bit





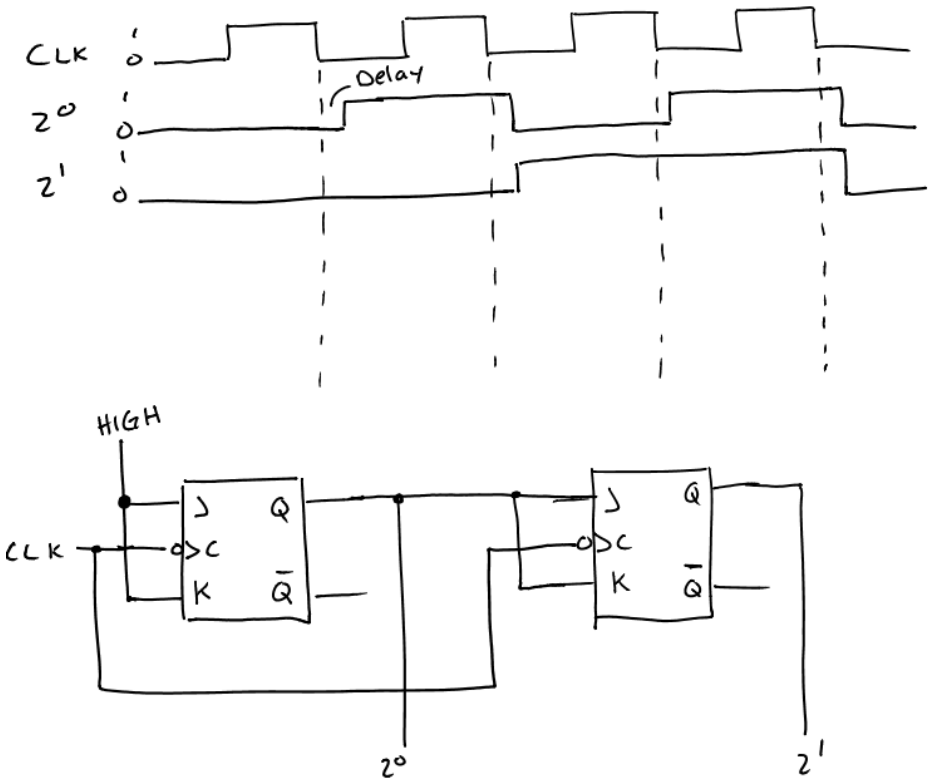
- Delay times accumulate in an Asynchronous Counter



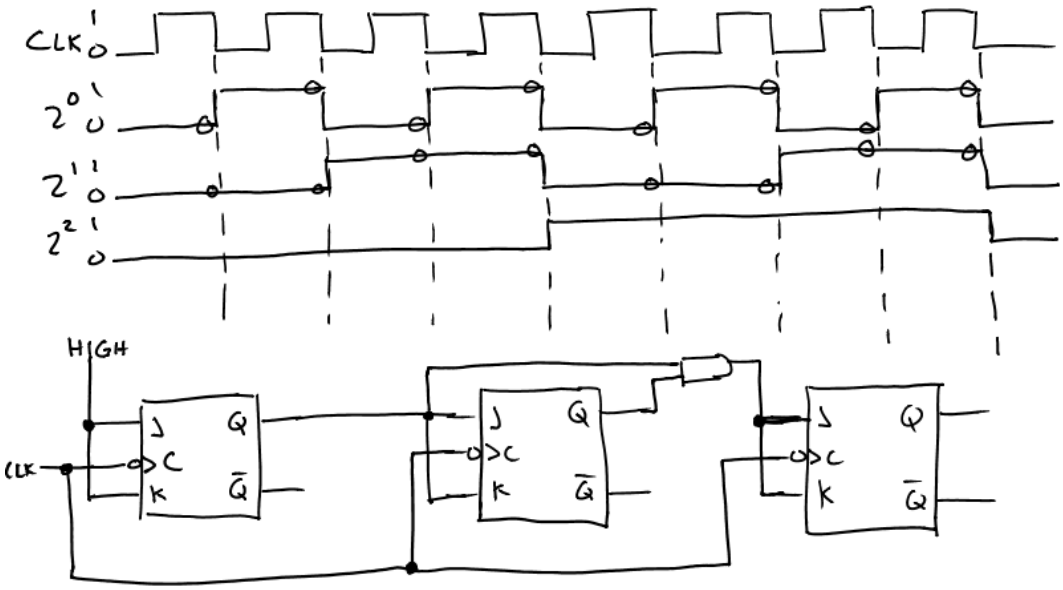
Synchronous Counters

- All Flip-Flops trigger off of the clock
- Utilize the propagation delay times

2-bit

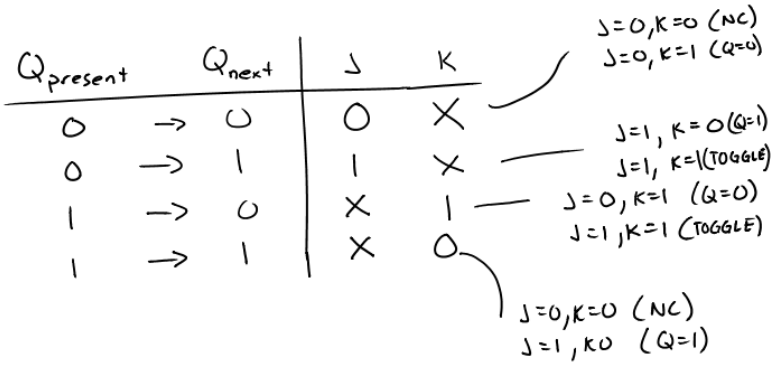


3-bit



Design of Synchronous Counters

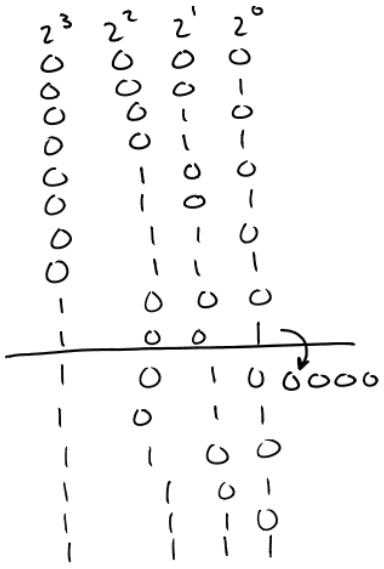
- Not all sequential circuits follow the weighted binary number system
- Gray Code
  - 000
  - 001
  - 011
  - 010
  - 110
  - 111
  - 101
  - 100
- Need to use Karnaugh Maps to design the input circuit for the J and K inputs of each Flip-Flop
- Design Components
  - Next State Table: Shows the current state and the state that follows
  - J-K Transition Table: Shows the values for J and K to achieve a transition in logic level for Q



  - Karnaugh Maps
  - Circuit Schematic

Counters with Truncated Sequences

- Count to a number less than the max



Modulus => Total number of states

4-bit => $2^4 = 16$

Truncated Sequence

Modulus < Max Modulus

Decade Counter

Modulus 10

0000 → 1001

0 → 9

Use the RESET ($\overline{R}_D$) of each Flip-Flop when 1010 occurs

RESET when $2^3 = 1$ AND $2^1 = 1$