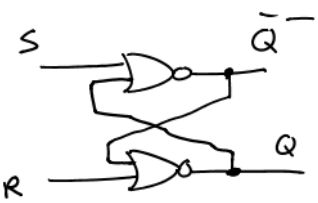
Flip-Flops

- Bistable Devices: Two stable output scenarios

S-R Latch



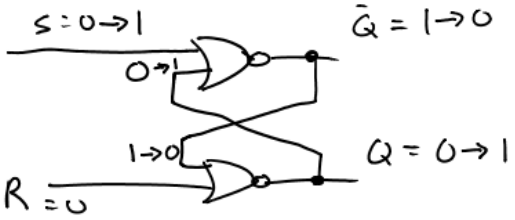
Normally => S = 0 & R = 0 until you want to change the state

S	R	Q	$\bar{Q}$	
0	0	NC	NC	No Change
1	0	1	0	SET (Q = 1)
0	1	0	1	RESET (Q = 0)
1	1	INVALID		

SET

Initially S = 0, R = 0, Q = 0, $\bar{Q}$ = 1

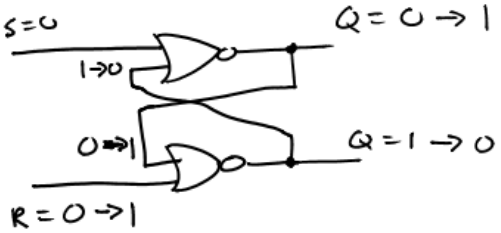
=> Apply a HIGH to S



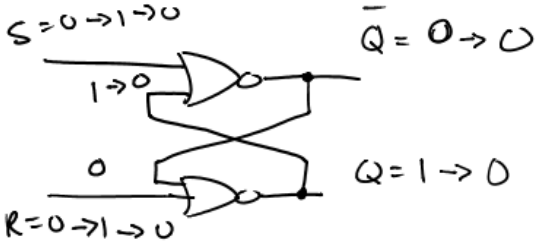
RESET

Initially: S = 0, R = 0, Q = 1, $\bar{Q}$ = 0

Apply a HIGH to R

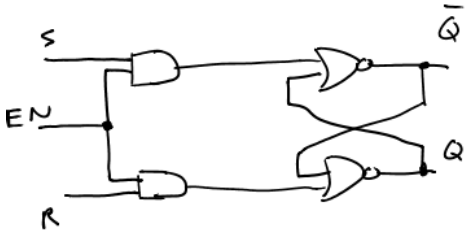


INVALID



Gated S-R Latch

- Adds an AND Gate that serves as an enabler

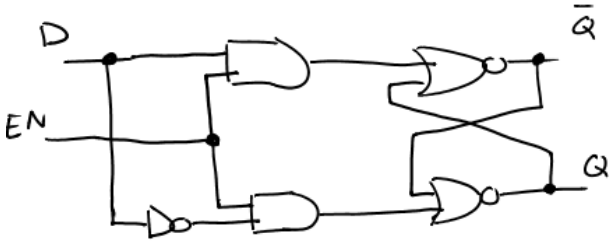


EN	S	R	Q	$\bar{Q}$	
0	X	X	NC	NC	No Change
1	0	0	NC	NC	
1	1	0	1	0	
1	0	1	0	1	
1	1	1	INVALID		

Gated D Latch

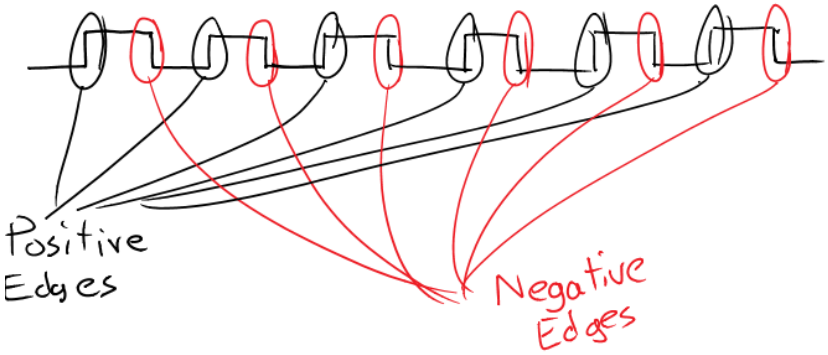
- One input and an enabler

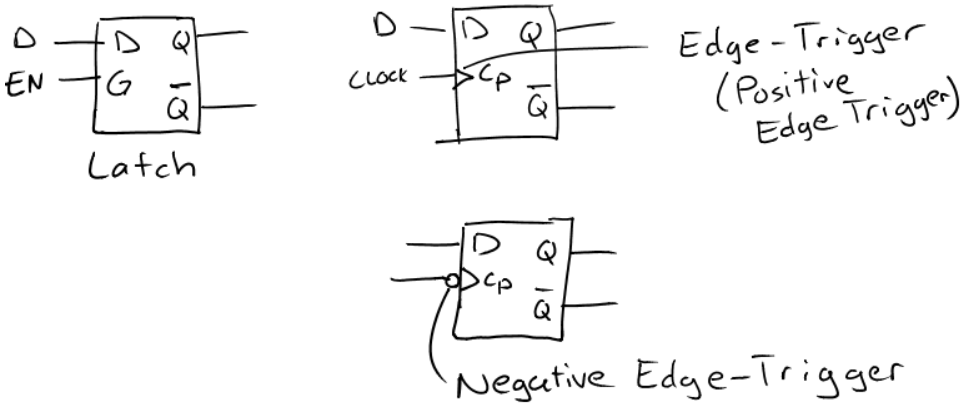
EN	D	Q	$\bar{Q}$	
0	X	NC	NC	
1	1	1	0	SET
1	0	0	1	RESET



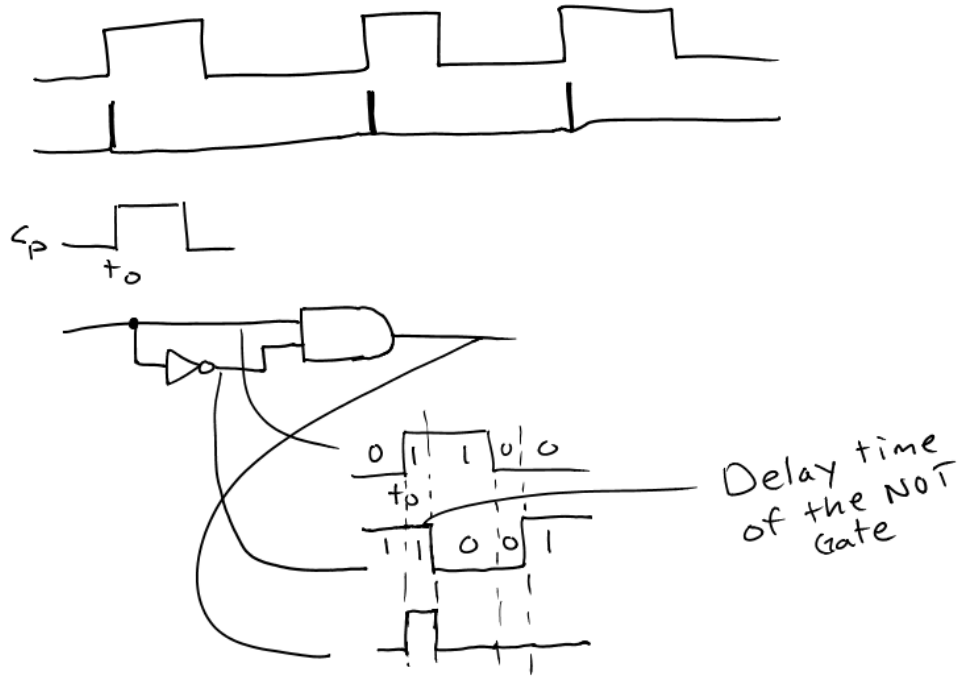
Edge-Triggered Flip-Flops

- The Flip-Flop is activated at either the positive or negative edges of a clock pulse
  - Latch: No edge trigger
  - Flip Flop: Edge trigger



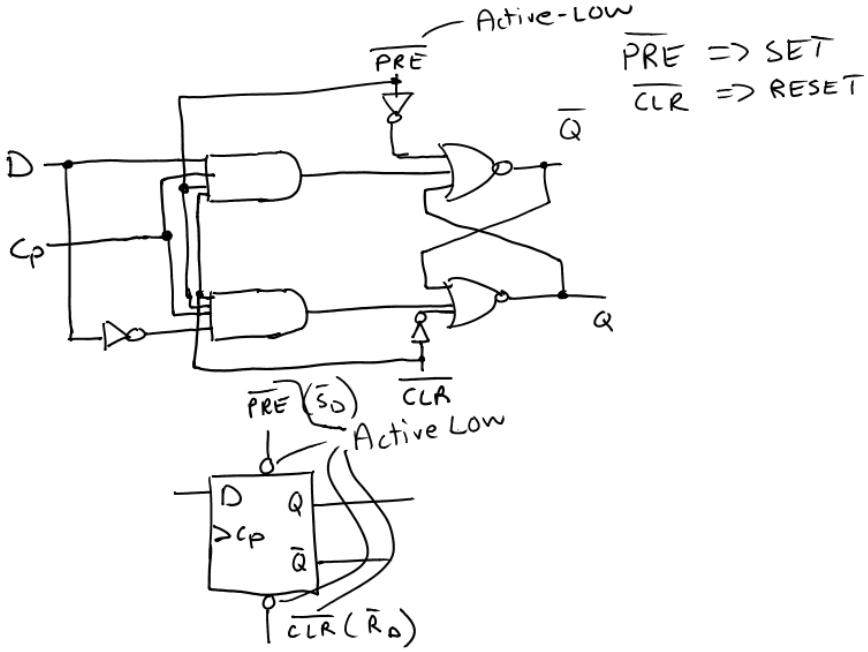


Edge Triggering



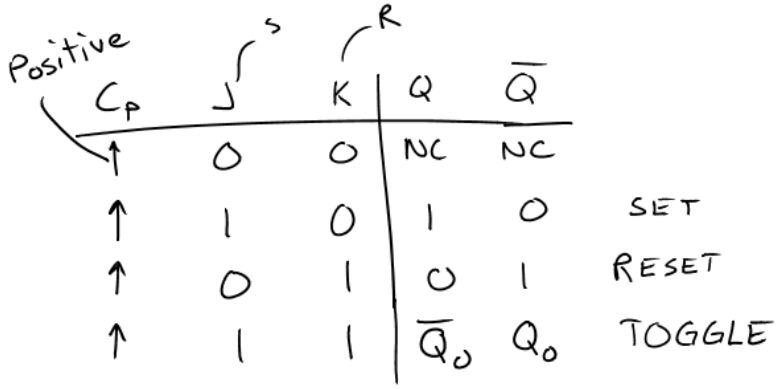
Asynchronous Inputs

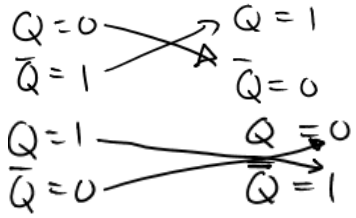
- Put the Flip Flop in SET or RESET independent of the clock

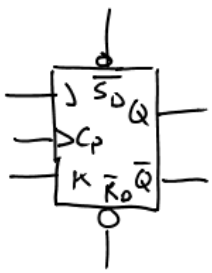


J-K Flip-Flop

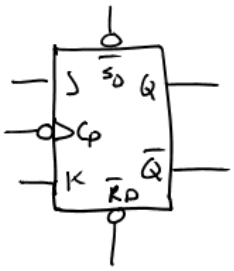
- Removes the invalid state of the S-R Latch







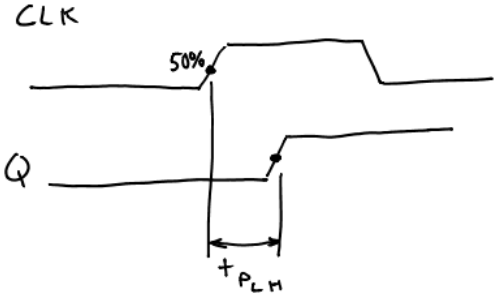
Positive Edge Trigger

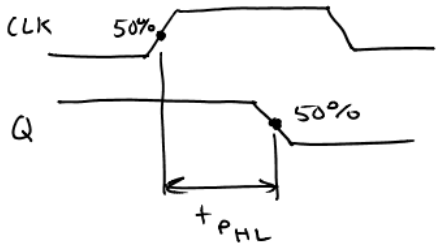


Negative Edge Trigger

Propagation Delay Times

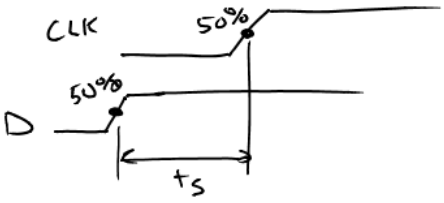
- Time delay due to the time needed for the circuit to change logic levels





Set Time

How long before the triggering the inputs need to be at the correct logic level.



Hold Time

How long the inputs must remain at the desired logic level after the triggering edge