Flip-Flops

- Bistable Devices: Two stable output scenarios

S-R Latch

\[
\begin{array}{c|c|c|c|c}
S & R & Q & \bar{Q} \\
\hline
0 & 0 & NC & NC \\
1 & 0 & 1 & 0 \\
0 & 1 & 0 & 1 \\
1 & 1 & INVALID & \\
\end{array}
\]

Normally \( S = 0 \) \& \( R = 0 \) until you want to change the state

**SET**

Initially \( S = 0 \), \( R = 0 \), \( Q = 0 \), \( \bar{Q} = 1 \)

\( \Rightarrow \) Apply a HIGH to \( S \)

**RESET**

Initially: \( S = 0 \), \( R = 0 \), \( Q = 1 \), \( \bar{Q} = 0 \)

Apply a HIGH to \( R \)
Gated S-R Latch
- Adds an AND Gate that serves as an enabler

<table>
<thead>
<tr>
<th>EN</th>
<th>S</th>
<th>R</th>
<th>Q</th>
<th>Q</th>
<th>¬Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>NC</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>NC</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>¬Q</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>IN</td>
<td>VA</td>
<td>LD</td>
</tr>
</tbody>
</table>

No Change

Gated D Latch
- One input and an enabler

<table>
<thead>
<tr>
<th>EN</th>
<th>D</th>
<th>Q</th>
<th>Q</th>
<th>¬Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>NC</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>SET</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>RESET</td>
</tr>
</tbody>
</table>

¬Q
Edge-Triggered Flip-Flops
- The Flip-Flop is activated at either the positive or negative edges of a clock pulse
  - Latch: No edge trigger
  - Flip Flop: Edge trigger

### Edge Triggering

- **Positive Edge-Trigger**
- **Negative Edge-Trigger**

- **Delay time of the NOT gate**

- **Latch**

- **Flip Flop**
Asynchronous Inputs
- Put the Flip Flop in SET or RESET independent of the clock

J-K Flip-Flop
- Removes the invalid state of the S-R Latch
**ENGR 2218 – Digital Logic**

**Flip-Flops**

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**Propagation Delay Times**
- Time delay due to the time needed for the circuit to change logic levels

**Set Time**
- How long before the triggering the inputs need to be at the correct logic level.

**Hold Time**
- How long the inputs must remain at the desired logic level after the triggering edge.